This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-37. (Cancelled)

38. (New) A system for evaluating parameters of a semiconductor wafer or wafer set comprising:

a source which generates a probe beam which is transmitted through a lens and onto a semiconductor wafer;

a detector which detects the probe beam after it is reflected off the semiconductor wafer, and the detector outputs signals based on the probe beam reflected of the semiconductor wafer;

a processor coupled to the detector to receive the signals; and

wherein the processor is operable to generate measurement data, based on the received signals, for multiple points on the semiconductor wafer or wafer set, and to define multiple domains, wherein a domain has corresponding measured data, and to determine an optimum group of parameter values for each domain, wherein to determine the optimum group for each domain the processor is operable to: associate different sets of theoretical semiconductor wafer parameter values with each domain; compare a first set of theoretical measurement data, derived from a first set of theoretical semiconductor wafer parameter values associated with a domain, to the measured data corresponding to the domain; and generate a new set of theoretical semiconductor wafer parameter values to be associated with the domain based on the comparing in a manner so as to associate increasingly more optimal theoretical semiconductor wafer parameter values with the domain, wherein the generation of the new set of theoretical semiconductor parameter values includes migrating at least one theoretical semiconductor parameter value from a set of theoretical semiconductor parameter values that has been associated with a different domain.

39. (New) The system of claim 38, wherein the processor is programmed such that the new set of theoretical semiconductor wafer parameter values are generated in accordance with a genetic algorithm.

40. (New) The system of claim 38, wherein the processor is programmed such that the processor generates a plurality of sets of theoretical semiconductor wafer parameter values, and derives a set of theoretical measurement data for each set of theoretical semiconductor wafer parameter values, and wherein the generating a plurality of sets of theoretical wafer parameter values includes defining a plurality of genotypes wherein a genotype includes a plurality of genes, wherein the plurality of genes correspond to different wafer parameters.

41. (New) The system of claim 40, wherein the processor is programmed such that one or more of the plurality of genes is defined as belonging to a first class where genes of the first class are optimized for each domain, and one or more of the plurality of genes is defined as belonging to a second class where genes of the second class are optimized across a plurality of domains, and one or more of the plurality genes is defined as belonging to a third class where genes of the third class are optimized across all domains, such that the genes of the third class are deemed to have the same value for each domain.

42. (New) The system of claim 40, wherein the processor is programmed such that each of the genes of the plurality of genes is defined as belonging to one class of a group of different gene classes, wherein the group of different gene classes includes a first class where genes of the first class are optimized for each domain, a second class where genes of the second class are optimized across a plurality of domains, and a third class where genes of the third class are optimized across all domains, such that the genes of the third class are deemed to have the same value for each domain.